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L6: Entry 2 of 10

File: USPT

Oct 21, 2003

US-PAT-NO: 6636986

DOCUMENT-IDENTIFIER: US 6636986 B2

TITLE: Output and/or input coordinated processing array

DATE-ISSUED: October 21, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Norman; Richard S.	Sutton			CA

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hyperchip Inc.	Montreal			CA	03

APPL-NO: 10/ 000813 [PALM]

DATE FILED: November 30, 2001

## PARENT-CASE:

This application is a continuation of U.S. application Ser. No. 09/679,168, filed on Oct. 4, 2000, now U.S. Pat. No. 6,408,402, entitled "Output And/Or Input Coordinated Processing Array" which is a continuation of U.S. application Ser. No. 09/376,194, filed on Aug. 18, 1999, now U.S. Pat. No. 6,154,855 entitled "Efficient Direct Replacement Cell Fault Tolerant Architecture" which is a continuation of U.S. application Ser. No. 08/821,672, filed Mar. 19, 1997, now U.S. Pat. No. 6,038,682 entitled "Fault Tolerant Data Processing System Fabricated on a Monolithic Substrate" which is a continuation of U.S. application Ser. No. 08/618,397 filed Mar. 19, 1996, now U.S. Pat. No. 5,748,872 entitled "Direct Replacement Cell Fault Tolerant Architecture" which is a continuation of U.S. application Ser. No. 08/216,262 filed Mar. 22, 1994, now abandoned, entitled "Efficient Direct Replacement Cell Fault Tolerant Architecture."

INT-CL: [07] H02 H 3/05

US-CL-ISSUED: 714/10; 714/48, 714/25

US-CL-CURRENT: 714/10; 714/25, 714/48

FIELD-OF-SEARCH: 714/10, 714/48, 714/25, 714/30, 714/29

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>2942193</u>	June 1960	Tyron	328/92
<input type="checkbox"/>	<u>3543048</u>	November 1970	Klaschka	307/204
<input type="checkbox"/>	<u>3860831</u>	January 1975	Tagami et al.	307/441
<input type="checkbox"/>	<u>3913072</u>	October 1975	Catt	346/172.5
<input type="checkbox"/>	<u>4591980</u>	May 1986	Huberman et al.	364/200
<input type="checkbox"/>	<u>4591981</u>	May 1986	Kassabov	364/200
<input type="checkbox"/>	<u>4617475</u>	October 1986	Reinschmidt	307/441
<input type="checkbox"/>	<u>4621201</u>	November 1986	Amdahl et al.	307/219
<input type="checkbox"/>	<u>4622632</u>	November 1986	Tanimoto et al.	364/200
<input type="checkbox"/>	<u>4698807</u>	October 1987	Marwoord et al.	395/182.09
<input type="checkbox"/>	<u>4709327</u>	November 1987	Hillis et al.	364/200
<input type="checkbox"/>	<u>4720780</u>	January 1988	Dolecek	364/200
<input type="checkbox"/>	<u>4798976</u>	January 1989	Curtin et al.	307/441
<input type="checkbox"/>	<u>4800302</u>	January 1989	Marum	307/441
<input type="checkbox"/>	<u>4855903</u>	August 1989	Carleton et al.	364/200
<input type="checkbox"/>	<u>4873626</u>	October 1989	Gifford	364/200
<input type="checkbox"/>	<u>4908751</u>	March 1990	Smith	364/200
<input type="checkbox"/>	<u>4933836</u>	June 1990	Tulpule	364/200
<input type="checkbox"/>	<u>4942517</u>	July 1990	Cok	364/200
<input type="checkbox"/>	<u>5056000</u>	October 1991	Chang	364/200
<input type="checkbox"/>	<u>5065308</u>	November 1991	Evans	395/182.02
<input type="checkbox"/>	<u>5208872</u>	May 1993	Sakuta et al.	365/230
<input type="checkbox"/>	<u>5267198</u>	November 1993	Hatano et al.	365/189.01
<input type="checkbox"/>	<u>5276648</u>	January 1994	Yanagisawa et al.	365/201
<input type="checkbox"/>	<u>5402377</u>	March 1995	Ohhata et al.	365/200
<input type="checkbox"/>	<u>5748872</u>	May 1998	Norman	395/182.09
<input type="checkbox"/>	<u>6154855</u>	November 2000	Norman	714/10

## OTHER PUBLICATIONS

Anonymous, "Diagonal Replacement Scheme to Recover Fault in a Mesh", Research Disclosure, Jan. 1990, p.70.

"RISC Drives PowerPC", BYTE, Aug. 1993, pp 79-90.

"Intel Launches Rocket in a Socket", BYTE, May 1993, pp. 92-108.

"Machines from the Lunatic Fringe,", TIME, Nov. 11, 1991, pp 74-75.

Chau et al "Fault Tolerance For Multistage Interconnection Networks" 1989 1992 pp 430-435.

Suginara et al "On Fault Tolerance of Reconfigure Arrays Using Spare Processors" 1991 IEEE pp 10-15.

Rudokas et al "A Digital Optical Imprementation of RISC" 1991 IEEE pp 436-441.

Caesar et al "A Processor Approach For Video Signal Processing" IEEE pp 57-60.

Bourbakis et al A RISC Architectural Design of the Hermes Multiprocessor Vision Machine 1988 IEEE 287-293.

Wang et al "Reconfiguration of VLSI/WSI Mech Array Process with Two-Level Redundancy" 1989-IEEE pp 547-554.

ART-UNIT: 2131

PRIMARY-EXAMINER: Wright; Norman M.

## ABSTRACT:

A data processing system containing a monolithic network of cells with sufficient redundancy provided through direct logical replacement of defective cells by spare cells to allow a large monolithic array of cells without uncorrectable defects to be organized, where the cells have a variety of useful properties. The data processing system according to the present invention overcomes the chip-size limit and off-chip connection bottlenecks of chip-based architectures, the von Neumann bottleneck of uniprocessor architectures, the memory and I/O bottlenecks of parallel processing architectures, and the input bandwidth bottleneck of high-resolution displays, and supports integration of up to an entire massively parallel data processing system into a single monolithic entity.

40 Claims, 32 Drawing figures

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File: USPT

Oct 21, 2003

DOCUMENT-IDENTIFIER: US 6636986 B2

TITLE: Output and/or input coordinated processing array

Detailed Description Text (17):

Accordingly, the fault tolerant monolithic data processing architecture in another embodiment of the present invention as shown in FIG. 3 combines one or more standard "mono-chip" RISC or CISC processors 380 fabricated on the same monolithic substrate 390 with the monolithic memory array 30 of memory cells 300 as described in the previous direct access memory embodiment of the present invention. While this will reduce the overall yield to the array's yield times that of the processor(s), it keeps all the processor/memory interconnections on a microscopic scale on a single monolithic region. This leaves the entire circumference of the whole region, which is considerably larger than that of a single chip, free for connections to other subsystems. Using this embodiment one can reduce the entire memory and processor subsystems of an advanced desk-top system (such as a 486 with 16 megabytes of main memory) to a single credit-card sized module. It is anticipated that arrays with defective processors can have those processors disabled and still be used as memory-only arrays, and that other functions, such bios chips 380', video accelerators 380", or I/O controllers 380'" could be integrated in addition to or instead of the processors(s).

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L7: Entry 1 of 3

File: USPT

Aug 27, 1985

US-PAT-NO: 4538247

DOCUMENT-IDENTIFIER: US 4538247 A

TITLE: Redundant rows in integrated circuit memories

DATE-ISSUED: August 27, 1985

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Venkateswaran; Kalyanasundaram	San Jose	CA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Fairchild Research Center	Mountain View	CA			02

APPL-NO: 06/ 457999 [PALM]

DATE FILED: January 14, 1983

INT-CL: [03] G11C 11/40

US-CL-ISSUED: 365/230; 365/200, 365/210

US-CL-CURRENT: 365/230.06; 326/106, 326/13, 365/200, 365/210

FIELD-OF-SEARCH: 365/189, 365/200, 365/210, 365/230

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

 

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4250570</u>	February 1981	Tsang et al.	365/210

ART-UNIT: 233

PRIMARY-EXAMINER: Fears; Terrell W.

ATTY-AGENT-FIRM: Silverman; Carl L. Carroll; David H. Colwell; Robert C.

## ABSTRACT:

Decoding apparatus for an integrated circuit memory having normal rows of memory cells 10 and at least one selectively connectable redundant second row of memory cells 31 for being connected in place of one of the first rows 10 includes a redundant decoder (transistors 32, 33. . . n) connected to each of the redundant rows 31, the redundant decoder including a plurality of selectable connections (F.sub.1, F.sub.2 . . . F.sub.n) for creating an address for each of the at least one redundant rows 31; a

control signal generating circuit (gates 45, 46, and 47) for generating a control signal of a first state until an address is supplied to the memory and of a second state if any of the redundant rows 31 are selected by the address, and another decoder (transistors 23 and 39) connected to receive control signal .phi..sub.C from the generating circuit for controlling normal rows 10 and the redundant row 31 in response thereto.

18 Claims, 3 Drawing figures

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L7: Entry 1 of 3

File: USPT

Aug 27, 1985

DOCUMENT-IDENTIFIER: US 4538247 A

TITLE: Redundant rows in integrated circuit memories

Brief Summary Text (6):

One prior art solution to this problem has been to design and fabricate integrated circuit memories using more fault tolerant designs and processes. This approach, by itself, does not always suffice. Consequently, another solution which has received increasing attention is the fabrication of redundant components on the same chip. At a suitable stage in the fabrication process, the non-functional portions of the circuit are replaced with the redundant portions, typically by using redundant wiring techniques, fuses, discretionary metal masks, or other techniques. The usual prior art approach, however, has been to replace an entire relatively large block in the memory with a new block. For example, in a 64 k memory divided into 16 sections, each of 4 k bits, a defective bit in a single section will result in the replacement of the entire 4 k section. Unfortunately, this approach requires a considerable amount of extra logic and extra space on the integrated circuit.